Amendments to the Specification:

Please replace the paragraph at page 1, line 21 through page 2, line 4 with the following amended paragraph:

When the $(2^n-1)$ comparators undergo a state transition, respective neighboring comparators also undergo a state transition. Here, by the layout method described above, a digital signal output from the neighboring comparators do not remain at ~~transit to~~ the same state but transit to a different state. As a result, since the neighboring comparators adjacent to the comparators affect operation of the comparators to thereby increase an offset voltage of the comparators, an accurate digital signal cannot be generated.

Please replace the paragraph at page 2, line 13 through page 3, line 5 with the following amended paragraph:

In order to achieve the above object, the preferred embodiments of the present invention provide a layout method of a comparator array of a flash type analog to digital converting circuit, the flash type analog to digital converting circuit including: (i) a reference voltage for generating $(2^n-1)$ voltages and being arranged to be folded; (ii) a comparator array including $(2^n-1)$ comparators for comparing voltage differences between the respective $(2^n-1)$ voltages and an analog input signal to generate a digital thermometer code ~~signal~~ having $(2^n-1)$ bits ~~thermometer codes~~; and (iii) an encoder for encoding the digital ~~signal having $(2^n-1)$~~ thermometer [[codes]] code having $(2^n-1)$ bits to generate an n-bit digital signal. According to the layout method, the comparators are arranged such that the comparators of $(2^n-1)^{th}$ comparator to $(2^n/2)^{th}$ comparator are arranged in order and the comparators of $(2^n/2-1)^{th}$ comparator to a first comparator are arranged in a reverse fashion between the comparators of the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator. The comparators are arranged such that the neighboring comparators adjacent to the respective $(2^n-1)$ comparators remain at ~~transit~~

[[to]] the same state when the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator transit to different states respectively.

Please replace the paragraph at page 3, lines 6 through 12 with the following amended paragraph:

Each of the $(2^n-1)$ comparators can include a positive input and output terminal and a negative input and output terminal, and the terminals of the comparators from [[of]] the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator are arranged in order of the positive input and output terminal, the negative input and output terminal, the negative ~~positive~~ input and output terminal, the positive ~~negative~~ input and output terminal, the negative input and output terminal, the positive input and output terminal, the positive ~~negative~~ input and output terminal, and the negative ~~positive~~ input and output terminal.

Please replace the paragraph at page 3, lines 13 through 20 with the following amended paragraph:

Alternatively, each of the $(2^n-1)$ number of comparators can include a positive input and output terminal and a negative input and output terminal, and the terminals of the comparators from [[of]] the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator can be arranged in order of the negative input and output terminal, the positive input and output terminal, the positive ~~negative~~ input and output terminal, the negative ~~positive~~ input and output terminal, the positive input and output terminal, the negative input and output terminal, the negative ~~positive~~ input and output terminal, and the positive ~~negative~~ input and output terminal.

Please replace the paragraph at page 3, line 21 through page 4, line 8 with the following amended paragraph:

The comparator array can include first and second dummy comparators, the first dummy comparator arranged adjacent to the $(2^n-1)^{th}$ comparator, the second dummy comparator arranged adjacent to $(2^n/2)^{th}$ comparator, wherein the comparators from [[of]] the first dummy comparator to the second dummy comparators include ~~includes~~ positive and negative input and output terminals, respectively, and the terminals of the comparators from [[of]] the first dummy comparator to the

second dummy comparators are arranged in order of the positive input and output terminal, the negative input and output terminal, the negative ~~positive~~ input and output terminal, the positive ~~negative~~ input and output terminal, the negative input and output terminal, the positive input and output terminal, the positive ~~negative~~ input and output terminal, and the negative ~~positive~~ input and output terminal.

Please replace the paragraph at page 4, lines 9 through 14 with the following amended paragraph:

The second dummy comparator can be configured such that a reference voltage and an analog input signal applied to the positive input terminal of the $(2^n/2-1)^{th}$ comparator are applied to the positive input terminal of the second dummy comparator, and a reference voltage and an analog input signal applied to the negative input terminal of the $(2^n/2-1)^{th}$ comparator are applied to the negative ~~positive~~ input terminal of the second dummy comparator.

Please replace the paragraph at page 4, line 15 through page 5, line 2 with the following amended paragraph:

The comparator array can include first and second dummy comparators, the first dummy comparator arranged adjacent to the $(2^n-1)^{th}$ comparator, the second dummy comparator arranged adjacent to $(2^n/2)^{th}$ comparator, wherein the comparators from [[of]] the first dummy comparator to the second dummy comparators include ~~includes~~ positive and negative input and output terminals, respectively, and the terminals of the comparators from [[of]] the first dummy comparator to the second dummy comparators are arranged in order of the negative input and output terminal, the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, and the negative input and output terminal.

Please replace the paragraph at page 5, lines 3 through 8 with the following amended paragraph:

The second dummy comparator can be configured such that a reference voltage and an analog input signal applied to the positive input terminal of the $(2^n/2-1)^{th}$ comparator are applied to

the positive input terminal of the second dummy comparator, and a reference voltage and an analog input signal applied to the negative input terminal of the $(2^n/2-1)^{th}$ comparator are applied to the negative ~~positive~~ input terminal of the second dummy comparator.

Please replace the paragraph at page 5, lines 9 through 19 with the following amended paragraph:

According to another aspect, the invention is directed to a layout method of a comparator array, comprising, among $(2^n-1)$ comparators for comparing voltage differences between each of $(2^n-1)$ voltages and an analog input signal to generate a digital signal having $(2^n-1)$ thermometer codes, (i) arranging the comparators such that the comparators of $(2^n-1)_{th}$ comparator to $(2^n/2)^{th}$ comparator are arranged in order and the comparators of $(2^n/2-1)^{th}$ comparator to a first comparator are arranged in a reverse fashion between the comparators of the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator; and (ii) arranging the comparators such that the neighboring comparators adjacent to the respective $(2^n-1)$ ~~number of~~ comparators remain at ~~transit to~~ the same state when the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator transit to different states respectively.

Please replace the paragraph at page 5, line 20 through page 6, line 3 with the following amended paragraph:

Each of the $(2^n-1)$ comparators includes a positive input and output terminal and a negative input and output terminal, and the terminals of the comparators from [[of]] the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator are arranged in order of the positive input and output terminal, the negative input and output terminal, the negative ~~positive~~ input and output terminal, the positive ~~negative~~ input and output terminal, the negative input and output terminal, the positive input and output terminal, the positive ~~negative~~ input and output terminal, and the negative ~~positive~~ input and output terminal.

Please replace the paragraph at page 6, lines 4 through 10 with the following amended paragraph:

Each of the $(2^n-1)$ comparators can include a positive input and output terminal and a negative input and output terminal, and the terminals of the comparators from [[of]] the $(2^n-1)^{th}$

comparator to the $(2^n/2)^{th}$ comparator are arranged in order of the negative input and output terminal, the positive input and output terminal, the positive ~~negative~~ input and output terminal, the negative ~~positive~~ input and output terminal, the positive input and output terminal, the negative input and output terminal, the negative ~~positive~~ input and output terminal, and the positive ~~negative~~ input and output terminal.

Please replace the paragraph at page 9, lines 4 through 5 with the following amended paragraph:

The encoder 30 encodes a digital thermometer code ~~signal~~ having $(2^n-1)$ ~~thermometer codes~~ bits outputted from the comparator array 20 to generate an n-bit digital signal.

Please replace the paragraph at page 11, lines 2 through 9 with the following amended paragraph:

For example, in the comparator C1, when the analog input signal transits from a level of REF- to VR1 to a level of VR1 to VR2, the digital signal of the negative output terminal transits from 1 to 0, and the digital signal of the positive output terminal transits from 0 to 1. At this time, the digital signal of the positive output terminal of the neighboring comparator C15 transits from 0 to 1 [[0]], and the digital signal of the negative output terminal of the neighboring comparator C14 transits from 1 to 0 [[1]]. That is, the digital signals outputted from the neighboring comparators C15 and C14 transit to different states.

Please replace the paragraph at page 11, lines 13 through 22 with the following amended paragraph:

For example, the comparator C1 should generate a digital signal of 1 and 0 when the analog input signal AIN has a level of REF- to VR1. But, in the case that an offset voltage exceeds an allowable range, the digital signal of 1 and 0 is generated even when the analog input signal AIN has a level higher than a level of REF- to VR1, and the digital signal of 0 and 1 is generated even when the analog input signal AIN has a level lower than a level of VR1 to VR2. That is, when the analog input signal AIN has a level of VR1 to VR2, the digital signal of 0 and 1 should be generated, but

the digital signal of 1 and 0 is generated. When the analog input signal AIN has a level of REF- to VR1, the digital signal of 1 and 0 should be generated, but the digital signal of 0 [[1]]and 1 [[0]] is generated.

Please replace the paragraph at page 13, line 4 through page 14, line 2 with the following amended paragraph:

But, since positions of the negative and positive input and output terminals of the comparators C1, C14, C3, C12, C5, C10 [[C14]], C7, and C8 are changed, positions of the digital signals outputted are also changed. That is, a digital signal outputted from the comparators C1, C14, C3, C12, C5, C10 [[C14]], C7, and C8 is 1 and 0 in table 1 but 0 and 1 in table 2, and 0 and 1 in table 1 but 1 and 0 in table 2.

Please replace the paragraph at page 14, lines 3 through 9 with the following amended paragraph:

As can be seen in table 2, when the digital signal outputted from the negative and positive output terminals of each of the comparators C1 to C15 transits from 0, 1 to 1, 0 and from 1, 0 to 0, 1, the digital signal outputted from the positive or negative output terminals of the neighboring comparators remains at ~~transits from 0 to~~ 0 or ~~from 1 to~~ 1. That is, the digital signal outputted from the positive or negative output terminals of the neighboring comparators adjacent to each of the comparators C1 to C15 remains at ~~transits to~~ the same state.

Please replace the paragraph at page 14, lines 10 through 20 with the following amended paragraph:

For example, in comparator C1, when the analog input signal transits from a level of REF- to VR1 to a level of VR1 to VR2, the digital signal of the negative output terminal transits from 1 to 0, and the digital signal of the positive output terminal transits from 0 to 1. At this time, the digital signal of the positive output terminal of the neighboring comparator C15 remains at ~~transits from~~

0 ~~to 0~~, and the digital signal of the positive output terminal of the neighboring comparator C14 ~~transits from~~ remains at 0 ~~to 0~~. That is, the digital signals of the positive output terminals of the neighboring comparators C15 and C14 remains at ~~transit to~~ the same state. Hence, an accurate digital signal can be generated because a phenomenon is prevented that the comparator C1 affects operation of the neighboring comparators C15 and C14 to thereby increase an offset voltage.

Please replace the paragraph at page 16, line 9 through page 17, line 5 with the following amended paragraph:

As can be seen in table 3, when the digital signal outputted from the negative and positive output terminals of each of the comparators C1 to C15 transits from 0, 1 to 1, 0 or from 1, 0 to 0, 1, the digital signal outputted from the positive or negative output terminals of the neighboring comparators remains at ~~transits from~~ 0 ~~to 0~~ or ~~from 1 to~~ 1. That is, the digital signal outputted from the positive or negative output terminals of the neighboring comparators adjacent to each of the comparators C1 to C15 remains at transits to the same state.

Please replace the paragraph at page 17, lines 6 through 16 with the following amended paragraph:

For example, in comparator C1, when the analog input signal transits from a level of REF- to VR1 to a level of VR1 to VR2, the digital signal of the negative output terminal transits from 1 to 0, and the digital signal of the positive output terminal transits from 0 to 1. At this time, the digital signal of the negative output terminal of the neighboring comparator C15 remains at ~~transits from~~ 1 ~~to 1~~, and the digital signal of the negative output terminal of the neighboring comparator C14 transits from 1 to 1. That is, the digital signals of the negative output terminals of the neighboring comparators C15 and C14 remains at ~~transit to~~ the same state. Hence, an accurate digital signal can be generated because a phenomenon is prevented that the comparator C1 affects operation of the neighboring comparators C15 and C14 to thereby increase an offset voltage.